UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS INC., MICRON TECHNOLOGY TEXAS LLC, Defendants.	Case No. 2:22-CV-203-JRG-RSP JURY TRIAL DEMANDED

PLAINTIFF NETLIST, INC.'S OPENING CLAIM CONSTRUCTION BRIEF

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I. Introduction

This Court previously construed all six of the asserted patents in *Netlist Inc. v. Samsung Electronics Co. Ltd. et al.*, Case No. 2:21-cv-463-JRG ("*Samsung I*"). *See generally* Ex. 7 (*Samsung I* Order). More than half of Micron's proposed constructions seek a do-over of the 14 terms this Court construed in *Samsung I*, rehashing arguments this Court has already rejected. For new terms, Micron's proposed constructions contradict the intrinsic evidence and Federal Circuit case law.[1]

II. U.S. Patent Nos. 8,787,060 and 9,318,160

A. "electrical communication" ('060, cls. 1, 11, 20, 29; '160 patent, cl. 1)

Term	Netlist	Micron
"die interconnect[s] in electrical communication with the . . . group of array dies and not in electrical communication with the . . . group of at least one array die"	Plain and ordinary meaning, that is, "electrical communication" is different from "electrical connection"	Plain and ordinary meaning, *i.e.*, does not require importing "data ports" limitation into the claim to require electrical communications (or lack of electrical communications) between the die interconnect(s) and the data ports of the array die(s).

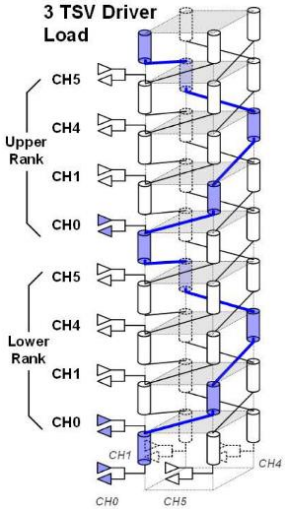
The claims of the '060 and '160 patents are directed to a memory package in which a claimed die interconnect is in "electrical communication" with one group of array dies in the memory package and "not in electrical communication" with a second group of array dies. For example, claim 1 of the '060 patent requires "at least a first die interconnect and a second die interconnect" and "the first die interconnect in ***electrical communication*** with the first group of array dies and ***not in electrical communication*** with the second group of at least one array die, the second die interconnect in ***electrical communication*** with the second group of at least one array die and not in electrical communication with the first group of array dies." '060 patent, 23:65-24:5.

Micron apparently equates "electrical ***communication***" with "electrical ***connection***," as Samsung did at the *Samsung I* trial. Ex. 23 (*Samsung I* Trial Tr.), at 1056:24-1057:7 (Samsung's expert

[1] All emphases are added unless stated otherwise.

Dr. Robins testifying that "the notion of electrical communication is a broad concept involving the transmission of electricity"); *see also* Ex. 9 (4/27 Ruekheim email) at 2 (Micron's counsel stating this term should be "construed as 'electrical communication' refers to ***coupling such that electricity can flow*** between the interconnects and the group of array dies").

Under Micron's interpretation, a die interconnect is in electrical communication with an array die so long as the array die is on the signal path. Hence, in the figure to the right, under Micron's interpretation, the interconnect annotated by the purple color would be in electrical communication with each array die, even though the interconnect is coupled to only drivers of CH0 dies and therefore cannot communicate data signals to memory circuitry of the other dies. The jury in *Samsung I* rejected such a non-infringement argument.



Ex. 10 at 2

Micron's interpretation is inconsistent with the intrinsic evidence. First, the claims and specification distinguish between the concept of "electrical communication" and "electrical connection." The claims recite "in electrical ***communication***"/"not in electrical ***communication***," and not "electrical ***connection***." *See* '060 patent, cls. 1, 11, 20, 29; '160 patent, cl. 1. And according to the specification, there can be "electrical connections leading from [a] TSV of the array dies that are not configured to be in electrical communication with [a] die interconnect," *e.g.*, as "stubs" that "are not configured to provide electrical communication with the memory cells of the array die." '060, 8:53-62.

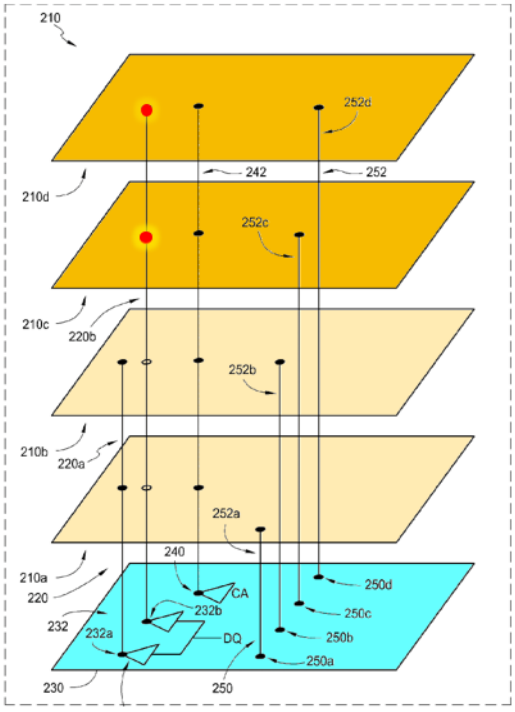
Second, the specification teaches that "electrical communication" and "not in electrical communication" concern what is between memory circuitry of an array die and die interconnect:

- "Each of the array die 210 may include one or more data ports . . . . The data ports enable ***electrical communication*** and data transfer ***between*** the corresponding

memory circuitry of the array dies 210 ***and a communication path way (e.g., a die interconnect)***."

- "[T]he die interconnects 220 may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect. For instance, die interconnect 220*b* may pass through array dies 210*a* and 210*b* using TSVs that do not enable ***electrical communication between the die interconnect 220b and data ports of the array dies 210a and 210b*** (illustrated by the unfilled circles). In this way the array dies 210*a*, 210*b* are not responsive to the data signal being[] transmitted by the die interconnect 220*b*. . . . In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent ***electrical communication between the die interconnect and the array die circuitry***. . . . ***[E]lectrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect*** may not exist or ***may be stubs***. These stubs are ***not configured to provide electrical communication with the memory cells of the array die***."

'060 patent at 5:41-45, 8:35-63; *see also* 6:3-8, 8:22-25, Fig. 2 (die interconnect 220b in electrical communication with array dies 210c-d, as shown by red dots, but not in electrical communication with 210a-b), Fig. 3 (320b in electrical communication with 310c-d but not in electrical communication with 310a-b). The above quotes make clear that a die is "not in electrical communication" when it is "not responsive to the data signal being transmitted by the die interconnect." *Id.*, 8:42-44. As already noted, an "electrical ***connection***" may exist without resulting in any "electrical ***communication***" between the die interconnect(s) and array die(s) by not "provid[ing] electrical communication with the memory cells of the array die." *Id.*, 8:53-62. Micron's proposed construction contradicts these disclosures and should thus be rejected.



'060, Fig. 2 (annotated)

B. "the second driver size being different from the first driver size" ('160 cl. 1)

Term	Netlist	Micron
"the second driver size being different from the first driver size"	Plain and ordinary meaning, that is, the size of the second driver being different from the size of the first driver	"the physical dimensions of the second driver being different from the physical dimensions of the first driver"

Netlist objects to Micron's proposed construction because it adds more ambiguity and does not resolve potential disputes. For instance, if the linear widths of composite transistors are the same (the length of the transistor is usually fixed by processing), but the number of transistors and/or the inter-transistor spacing is different, does that meet Micron's proposed construction? *E.g.*, '060, 17:43-45 ("The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver."). Or, if the width of each composite transistor differs but the driver circuit occupies the same space, does that meet Micron's proposed construction? *Id.* Micron's proposed construction does not say.

Micron's expert Dr. Stone opines that the addition of "physical dimensions" is necessary to distinguish "driver size" from "driver strength." Ex. 8 (Stone Decl.) ¶ 39. But in IPR, Micron points to "driver strength" as satisfying the "driver size" claim limitations. Ex. 11 (IPR2023-00883 Pet.) at 48 ("[A] POSITA would have been motivated by Wyman (in the combination of Ground 1, pp.32-34) to use ***drivers of different strengths*** (i.e., ***'first drivers' having a 'first driver size' and 'second drivers' having a 'second driver size'***) . . . ."). A party may not advance one position for validity and another for infringement. *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003) ("It is axiomatic that claims are construed the same way for both invalidity and infringement.").

Dr. Stone points to embodiments in the specification that discuss the size(s) of the drivers using terms such as "smaller" or "larger," or that discuss the "transistor size(s)" or "number of transistors" of the drivers, but none of these embodiments limit the plain language of claim 1. Ex. 8 (Stone Decl.) ¶ 42 (citing '160, 2:10-17, 13:13-26, 17:14-25). "[E]ven when the specification describes

only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Hill-Rom Services, Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372 (Fed. Cir. 2014) (citations omitted). Micron can point to no such words here, so its proposed construction should be rejected.

C. Claim 7 of the '060 Patent Is Not Indefinite

Term	Netlist	Micron
7. The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are ***selected in consideration of a load*** of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die.	Not indefinite	Indefinite

Micron argues that claim 7 of the '060 patent is indefinite because it recites both a system ("[t]he memory package of claim 1") and a step that is to be performed on that system ("wherein a first number of array dies . . . and a second number of at least one array die . . . are ***selected in consideration of a load***"). Micron cannot meet its burden to prove by clear and convincing evidence that claim 7 of the '060 patent is indefinite. *Sonix Tech. Co. v. Publ'ns Int'l*, 844 F.3d 1370, 1377 (Fed. Cir. 2017) ("Indefiniteness must be proven by clear and convincing evidence.").

Claims that recite both a system and a method for using that system are invalid as indefinite under § 112, ¶ 2. *IPXL Holdings, L.L.C. v. Amazon.com, Inc.* 430 F.3d 1377, 1384 (Fed. Cir. 2005). In *IPXL*, the Federal Circuit upheld as indefinite a dependent claim that required a specific method step by a user in addition to the system itself. *Id.* (finding indefinite claim that recited "[t]he system of claim 2 [including an input means] wherein the predicted transaction information comprises both a transaction type and transaction parameters associated with that transaction type, ***and the user uses***

the input means. . . ."). The Federal Circuit observed that the claim failed to communicate to a POSITA whether infringement occurred when a system with that capability was sold or when a user utilized that capability. *Id.* Such a problem does not exist here because the selection is part of the design process (*e.g.*, '060 patent, 11:12-30, 11:66-12:12, 14:4-39), and infringement occurs when the memory packages with the recited features are made, sold, used, or imported. *See KIPB LLC v. Samsung Elecs. Co. Ltd.*, No. 2:19-cv-56, 2020 WL 1495231, *6-*7 (E.D. Tex. Mar. 26, 2020) (claim reciting "the device as claimed in claim 1, wherein the parasitic capacitance between said gate and bulk silicon substrate ***is reduced by selecting*** the thickness of said second oxidation layer to be between 20 nm and 800 nm" was not indefinite under *IPXL* because the "language in question ***is directed toward the design criteria of the structure and its capabilities***, not the subsequent use of the product").

The Federal Circuit has also explained that claims are not indefinite if they "merely use permissible functional language to describe the capabilities of the claimed system." *Mastermine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1316 (Fed. Cir. 2017). In *Mastermine*, the Federal Circuit reversed the district court's finding of indefiniteness for a claim reciting "[a] system comprising . . . a reporting module . . . wherein the reporting module installed within the CRM software application ***presents*** a set of user-selectable database fields as a function of the selected report template, ***receives*** from the user a selection of one or more of the user-selectable database fields, and ***generates*** a database query as a function of the user selected database fields." *Id.* at 1315-16. The "active verbs" recited as part of the dependent claim at issue "represent[ed] permissible functional language used to describe capabilities of the 'reporting module.'" *Id.*

Here too, Claim 7 of the '060 patent uses "selected in consideration of a load" to describe a configuration of the "memory package." This is also analogous to *Gesture Tech. Partners, LLC v. Huawei Device Co.*, where this Court held that a claim reciting "[a] handheld device comprising . . . a first camera ***oriented to view*** a user of the handheld device and having a first camera output" was not indefinite

because "[t]he disputed term relates to configuration of the recited first camera rather than, for example, any user action or any action performed by or on the camera." No. 2:21-CV-40, 2021 WL 4760632, at *23 (E.D. Tex. Oct. 12, 2021). Likewise, claim 7 of the '060 patent does not require a user of the product to do any "selecting," but is instead directed to "the formation of a particular structure to have certain capabilities, which does not cause the problems identified in *IPXL*." *KIPB*, 2020 WL 1495231 at *6.

III. U.S. Patent No. 10,860,506

A. "one or more previous operations" ('506, cls. 1-3, 11, 15, 16)

Term	Netlist	Micron
"one or more previous operations"	one or more previous memory operations	"one or more previous memory operations" where "memory operations" are different from leveling operations

The parties agree that the term "one or more previous operations" means "one or more previous memory operations." The dispute is really what Micron means by "leveling operations" that differ from the memory operations. Specifically, Micron justifies its proposed construction based on arguments that Netlist allegedly made in pending IPRs involving the '506 patent and its grandparent, U.S. Pat. No. 9,824,035. *See* Dkt. 69-2 at 4 ("Micron is making this argument only to the extent that Netlist is successful in IPR2022-00236 or IPR2023-00205 where Netlist argued that leveling is not a memory operation."). The assertion is factually incorrect as to IPR2023-00205 where Netlist has not filed any substantive papers.

This assertion also mischaracterizes Netlist's arguments in IPR2022-00236, which does not involve the '506 patent. There, Netlist is arguing that the Tokuhiro reference does not disclose "obtain[ing] timing information based on one or more signals received by the each respective buffer circuit during a second memory operation," as required by claim 1 of the '035 patent. *See, e.g.*, Ex. 12 (IPR2022-00236 POR) at 20-29. To satisfy this limitation, Micron points to Tokuhiro's write leveling,

which Micron has conceded refers only to the known write leveling mode of the DDR3 standard, JESD79-3. *Id.* at 15, 18-19 (quoting Micron's expert's testimony: "Q. You're not offering any opinion that Tokuhiro teaches write leveling other than what is disclosed in DDR3 standard JESD79-3? A. That's correct."). This is consistent with the specification's distinguishing conventional DDR3 write leveling. *See* '506 patent, 15:21-23; *see also* 2:28-31 (referring to conventional leveling techniques); Ex. 13 at 63-64 (write leveling feature added in DDR3).

That is, Netlist at most only distinguished the prior DDR3 write leveling technique discussed in JESD79-3 from "memory operations." This is consistent with the specification's teachings that "memory operations" are understood to be operations performed by the memory module in response to memory commands. *See* '506 patent, 3:29-34 ("The memory module is operable to perform ***memory operations in response to memory commands*** (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module."). Tokuhiro's memory controller performs the write leveling function, not in response to a memory command, but only in response to data strobe and clock signals. Ex. 22 (Tokuhiro), 13:16-29, Fig. 7.

B. "determining" (506, cl. 14)

Term	Netlist	Micron
"before receiving the input C/A signals corresponding to the memory read operation, determining the first predetermined amount based at least on signals received by the first data buffer"	The step of "determining the first predetermined amount based as least on signals received by the first data buffer" occurs before the earlier recited step of "receiving . . . input C/A signals"	"during one or more previous memory operations, determining the first predetermined amount based at least on signals received by the first data buffer" where "memory operations" are different from leveling operations

Micron argues, as Samsung did in the *Samsung I* case, that the "determining" step of '506 claim 14 must occur "during one or more previous memory operations." The Court rejected this argument

in *Samsung I*, agreeing with Netlist that the claim simply requires that the step of "determining the first predetermined amount based as least on signals received by the first data buffer" occurs before the earlier recited step of "receiving . . . input C/A signals." Ex. 7 at 15-16, 35. The Court's construction was supported by the prosecution history, during which Netlist amended claim 2 (now claim 1) to include "during one or more previous operations" but did not add this language to claim 15 (now claim 14). *See id.* at 16; Ex. 14 (2020-10-16 Amendment After Notice of Allowance) at 2-7 (no amendment to claim 15). The Court's construction from *Samsung I* should control.

Moreover, Micron's attempt to read "write leveling" into the construction of this term is improper for all the reasons stated in Part III.A, and because the claim does not require that the "determining" step occur "during one or more previous operations."

IV. U.S. Patent No. 10,949,339

A. The "drive" terms ('339, cls. 1, 11, 19, 27)[2]

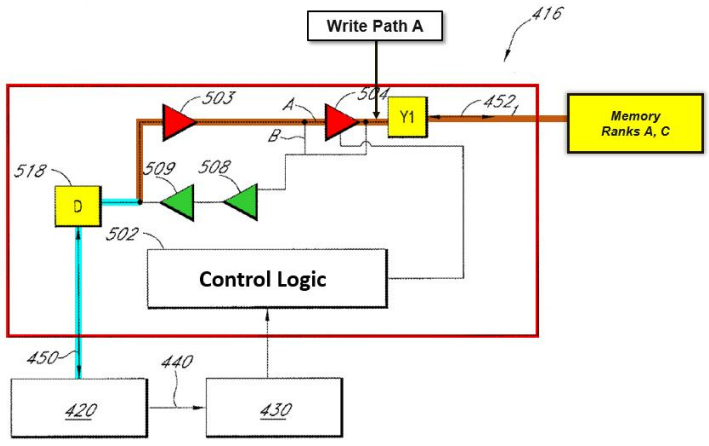
Term	Netlist	Micron
"to actively drive a respective byte-wise section of the N-bit wide write data"	to "drive" means "enabling only one of the data paths while the other possible paths are disabled" (i.e., no further construction necessary)	Adopts and applies the Court's adoption of the "fork-in-the-road" configuration and rejection of the "straight-line" configuration to construe "drive" to mean "enabling only one of the data paths while the other possible paths are disabled," *i.e.*, "enable only one of the data paths ***for the respective byte-wise section of the N-bit wide write data*** while the other possible data paths ***for the same respective byte-wise section of the N-bit wide write data*** are disabled"

In *Samsung I*, the Court construed "drive" to mean "enabling only one of the data paths while the other possible paths are disabled." Ex. 7 at 34. Micron argues that the Court should disregard its prior construction and instead hold (1) that the claims do not cover a "straight-line" configuration and (2) that the claim requires enabling only one of the data paths "for the respective byte-wise section of

[2] Claim 1 of the '339 patent is representative of the parties' dispute regarding the "drive" terms.

the N-bit wide write data" while the other possible data paths "for the same respective byte-wise section of the N-bit wide write data" are disabled. These arguments should be rejected.

"Straight line" and "fork in the road" are not terms that have any meaning to the jury, and Micron's proposed construction just replaces one term that needs construction with another. In *Samsung I*, the parties disputed whether the claims were limited to a "fork-in-the-road" configuration with multiple data paths where not all ranks of memory devices share a common data path, or whether the claims could also cover a "straight-line" configuration with multiple ranks of memory devices along the same data path. *See Samsung* I, Dkt. 76 at 4. Netlist explained that the claims do not require that there necessarily be an alternative second path and that the specification discloses embodiments with multiple ranks coupled to a single path, for example, two-rank embodiments with a single data path. Figs. 1A-2B; Dkt. 76 at 5-8; Dkt. 87 at 6-9. The specification identifies the need for load reduction even for two-rank memory modules ('339 patent, 4:48-5:3) and expressly states that the inventive load-reducing memory module architecture is compatible with two ranks. *Id.*, 9:44-49 ("[E]mbodiments with less than four ranks (e.g., one rank, ***two ranks*** . . . per memory module [] ***may be employed***."); 4:48-5:3 (identifying the need for load reduction even for two-rank memory modules), 16:45-54 (write and read buffer provide the load reduction). "Fork-in-the-road" is also not required for load reduction since load reduction is achieved with the use of write buffer 503 and read buffer 509. 16:45-47; *see also* modified Fig. 5 (right), where there are two ranks in each path even though a single load is presented to the system, 16:40-44



'339, Fig. 5 (modified configuration for two-rank DIMM)

(noting that operations of multiplexer 508 and read buffer 509 "may be split over two tristate buffers," as depicted in modified Fig. 5). The prosecution history is no different, where the discussion refers to opening and closing the same paths, not switching between different paths. *See* Ex. 7 at 9. The plural form "data paths" is used because there may be up to 8 individual paths for 8 bits of data.

The Court's claim construction order in *Samsung I* correctly recognized that the claims are not limited to multi-fork configurations. Ex. 7 at 10. The Court noted, for example, that "when" there exists a multi-fork configuration—meaning such a configuration does not necessarily have to exist—only one of the prongs of the fork is enabled at a given time:

> Based on this intrinsic record, the Court adopts the so-called fork-in-the-road approach. A skilled artisan would understand "driving" data from one side of the buffer to the other means, ***when there are multiple paths in a buffer through which that data can be driven***, enabling only one of the data paths while the other possible paths are disabled.

Id. at 10. That is, the Court construed "drive" as "enabling only one of the data paths while the other possible paths are disabled" with the phrasing "the other possible paths" accounting for the possibility that there are no alternative paths, *e.g.*, in a "straight-line" configuration. *Id.* Micron is thus incorrect that the Court rejected the "straight-line" configuration.

Micron also urges the Court to further construe the term "drive" in '339 cl. 1 as "enabl[ing] only one of the data paths ***for the respective byte-wise section of the N-bit wide write data*** while the other possible data paths ***for the same respective byte-wise section of the N-bit wide write data*** are disabled." *See* Dkt. 69-2 at 6-10; *see also id.* at 10-22 (similar proposed constructions of "drive" for each independent claim of the '339 patent). During meet and confer, Micron did not identify any need for additional construction of the "drive" terms. Micron's construction would exclude preferred embodiments shown in Figures 3B and 4B, where a byte-wise section of the N-bit wide data is transferred over two 4-bit paths, and not one path. *See also* '339 patent, 13:54-63 ("[A]s schematically illustrated by FIG. 4B (which corresponds generally to FIG. 3B), the data transmission circuits 416

may have a first bit width (e.g., a bit width of 8 bits) and the memory devices 412 may have a second bit width which is less than the first bit width (e.g., one-half the first bit width, or a bit width of 4 bits).").

In accordance, the Court's *Samsung I* order did not require any specific data paths that has to be enabled or disabled. *See* Ex. 7 at 9-10. Rather, the Court recognized that "the claimed invention, unlike the cited prior art, is about selectively opening otherwise closed data paths." Ex. 7 at 9 (analyzing prosecution history, including applicant's argument that "[t]his claimed limitation . . . is about controlling the data paths between the memory devices and the bus interface so that the data paths are open for a time period to allow data to be driven between the memory devices and the memory controller"); *see also* Ex. 7 at 10 ("'driving' data from one side of the buffer to the other means, ***when there are multiple paths in a buffer*** through which that data can be driven, enabling only one of the data paths while the other possible paths are disabled"). The Court's prior construction is sufficient and no further addition is required.

V. U.S. Patent Nos. 11,016,918 and 11,232,054

A. This Court's Constructions from *Samsung I* Should Apply in this Action

1. "a second plurality of address and control signals" ('918 cls. 1-3, 4-7, 9-13, 15, 21)

Term	Netlist	Micron
"a second plurality of address and control signals"	plain and ordinary meaning (i.e., no further construction necessary)	"a second plurality of address and control signals ***that are distinct from*** a first plurality of address and control signals"

In *Samsung I*, the Court construed "a second plurality of address and control signals" according to its plain and ordinary meaning. Ex. 7 at 35. Claim 1 of the '918 patent recites an "at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices." '918 patent, cl. 1. The Court explained that while the claim requires

that the "signal paths" for the first and second pluralities of address and control signals are distinct, "the amplitude and shape of the signals ***can be the same***." Ex. 7 at 26. Nothing in the claims or specification precludes the two sets of signals from being the same. *See, e.g.*, 38:46-47 (claim 1), 40:35–36 (claim 21), Figs. 12-14 (depicting control/address signals as input and output from switch 1052, both labeled "ADDR/CONT"), Fig. 15A-C (identically labeled "address/control" signals input to and output from register 1160). Micron has offered no reason to revisit the Court's construction from *Samsung I*.

2. "dual buck converter"/"dual-buck converter" ('918, cls. 2, 17, 28; '054, cl. 15)

Term	Netlist	Micron
"dual buck converter" / "dual-buck converter"	"a buck converter with two regulated voltage outputs" (i.e., no further construction necessary)	"buck converter with two outputs outputting two distinct regulated voltages"

The Court also previously rejected Micron's argument that the "dual buck converter" limitation requires two distinct voltages with distinct voltage amplitudes. Ex. 7 at 19-21, 34. The specification discloses that a buck converter outputs two regulated voltages to the memory system 1010 and discloses embodiments where both voltage 1104 and voltage 1105 of dual-buck converter 1124 could have the same amplitude, such as when both the isolation device and the FPGA operate at the same voltages. '918 patent, 29:44-50; Ex. 15 at 2 (examples of Xilinx FPGAs operating at same 2.5V voltage as isolation device disclosed in '918 patent, 29:44-50); *see also* Fig. 16, 29:18-31. The Court confirmed that Samsung failed to show that the specification expressly redefines "dual buck converter," and thus correctly found that the term should be construed to mean "a buck converter with two regulated voltage outputs," rejecting the argument that the voltage amplitudes cannot be the same. Ex. 7 at 19-21, 34.

3. "regulated voltage" / "voltage amplitude" ('918, all asserted claims)

Term	Netlist	Micron
"first" / "second"	plain and ordinary	"first regulated voltage ***that is distinct from*** the

/ "third" / "fourth" "regulated voltage"	meaning (i.e., no further construction necessary)	second, third, and fourth regulated voltages" / "second regulated voltage ***that is distinct from*** the first, third, and fourth regulated voltages" / "third regulated voltage ***that is distinct from*** the first, second, and fourth regulated voltages" / "fourth regulated voltage ***that is distinct from*** the first, second, and third regulated voltages"
"first" / "second" / "third" / "fourth" "voltage amplitude"	plain and ordinary meaning (i.e., no further construction necessary)	"first voltage amplitude ***that is distinct from*** the second, third, and fourth voltage amplitudes" / "second voltage amplitude ***that is distinct from*** the first, third, and fourth voltage amplitudes" / "third voltage amplitude ***that is distinct from*** the first, second, and fourth voltage amplitude" / "fourth voltage amplitude ***that is distinct from*** the first, second, and third voltage amplitude"

The Court previously construed the "regulated voltage" and "voltage amplitude" terms according to their plain and ordinary meaning. Ex. 7 at 34. The Court rejected Samsung's position that the terms "first," "second," "third," or "fourth" required each "regulated voltage" or "voltage amplitude" to have a different value. *Id.* at 23-24. The Court found that when read in the context of the claims, the terms "first," "second," "third," and "fourth" are "simply labels of convenience." *Id.* at 24 (further noting that "first regulated voltage" refers to "the voltage at the output of the 'first buck converter,'" and that the "'first voltage amplitude' is simply the amplitude at that output"). As for the "regulated voltage" terms, the claims merely require physically separate "regulated" voltage outputs, as the Court found. Ex. 7 at 24 (noting that "[t]he regulated voltages are distinct in the sense they are voltages at different physical outputs . . . .").

The Court's construction in *Samsung I* is consistent with the intrinsic evidence. For example, claim 1 of the '918 patent requires "a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes." '918 patent, 38:49-52. This limitation already requires that the second and fourth voltage amplitudes differ from each other. Micron's construction would render this limitation redundant, and is thus improper. Further, nothing in the

specification limits these terms. In a preferred embodiment, volatile memory 1032 and nonvolatile memory 1042 are both powered by a 1.8V first voltage 1102 produced by the buck-converter of sub-block 1122. '918 patent, 29:39-44, Fig. 16. But in another embodiment, "the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102." *Id.*, 29:61-64. In other words, both the volatile memory 1032 and nonvolatile memory 1042 can be powered by independent 1.8V voltages, suggesting that independent voltages need not have different voltage levels. In *Samsung I*, Netlist also explained power or current load considerations could justify the use of different voltage converters to generate the same voltage amplitude, similar to the common knowledge of plugging microwaves into different wall outlets of the same voltage. Ex. 16 (*Samsung I* Markman Hearing Tr.) at 23:24-25:8; *see also* '918 patent, 29:39-44 (using one converter to supply 1.8V to different components is for a load condition of 1.8V and 2.0A; more converters could be used for higher loads). Micron's construction for these terms should thus be rejected.

4. "at least three regulated voltages"/"plurality of regulated voltages" ('054, cls. 1, 16, 24)

Term	Netlist	Micron
"at least three regulated voltages"	plain and ordinary meaning (i.e., no further construction necessary)	"at least three ***distinct*** regulated voltages"
"plurality of regulated voltages"	plain and ordinary meaning (i.e., no further construction necessary)	"plurality of ***distinct*** regulated voltages"

As with the "regulated voltage" / "voltage amplitude" terms, the Court construed these claims according to their plain and ordinary meaning and rejected Samsung's attempt to read "distinct" into the claim language. Ex. 7 at 25. Micron's attempt to do so should be rejected for the same reasons.

5. "pre-regulated input voltage" / "input voltage" ('918, cls. 16-22, 30)

Term	Netlist	Micron
"pre-regulated input voltage" / "input voltage"	plain and ordinary meaning (i.e., no further construction necessary)	plain and ordinary meaning, where "a pre-regulated input voltage" is different from "an input voltage"

The parties' dispute centers around whether the "pre-regulated input voltage" recited by, *e.g.*, '918 claim 16 needs to be "different" from the claimed "input voltage." The Court rejected this argument in *Samsung I*. There, Samsung argued that "[b]ecause the '918 patent claims require both 'a pre-regulated input voltage' and 'an input voltage,' they are ***presumed to have different meanings***." *Samsung I*, Dkt. 82 at 9. The Court noted Samsung's argument, and found it unpersuasive:

> Samsung makes two arguments for its position. First, it relies on language from Claim 16 that requires "a voltage monitor circuit configured to monitor an input voltage" at the edge connections. Dkt. No. 82 at 5. According to Samsung, something must convert that input voltage into the "pre-regulated input voltages" received by the buck converters. . . .
>
> Neither argument is persuasive. ***Notably, the disputed term is a small part of the "buck converter" limitations and gives context to what the buck converters do—that is, receive an input voltage and produce an output voltage***. And although the claims characterize the input voltage into the buck converters as "pre-regulated" and the output voltages as "regulated," they impose no further limitations on the buck converters or, for that matter, the memory module.

Ex. 7 at 22. As the Court correctly observed, the language of the claims only requires that the "pre-regulated input voltage" be the input to the conversion circuits. *See, e.g.*, '918 patent, 39:60-61 ("first, second, and third buck converters configured to receive a pre-regulated input voltage"), 39:63-64 ("a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage.").

The specification likewise does not support Micron's position that the claimed "pre-regulated input voltage" must be different from "the input voltage received via a first portion of the plurality of edge connections." While a preferred embodiment in Fig. 16 teaches that pre-regulated voltages can be generated on-board from an input system voltage (28:39-58), the claims do not require that, as the Court's order explained. *See* Ex. 7 at 22 ("Although the written description discloses such structure (e.g., first and second power elements 1130, 1140), the claims do not require it."). "[E]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively

unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Hill-Rom*, 755 F.3d at 1372 (citations omitted). The specification teaches that a pre-regulated input voltage can be generated by *e.g.*, a second power supply. *E.g.*, Fig. 16 (element 1140 which would be understood to correspond to the second power supply in Fig. 12), 27:65-28:2. The second power supply 1080 need not be on the same printed circuit board 1020 as the memory module, but can instead be tethered to it. '918 patent, 26:30-35. Thus, with the voltage regulators on the same PCB as the memory devices and the second power supply being tethered to the memory module PCB, the pre-regulated input voltage that Micron points to could be supplied from off-board and as an input voltage received via edge connections. Micron's construction should thus be rejected.

6. "A memory module" ('918/'054, all asserted claims)

Term	Netlist	Micron
"A memory module"	The preamble is limiting	The preamble is non-limiting

In *Samsung I*, the Court agreed with Netlist that the preambles of the '918/'054 patents are limiting because they provide antecedent basis for the later-recited "memory module." Ex. 7 at 26-28, 35; *see also* '918 patent, 38:18-24 (PCB interface "including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system"), 39:53-59 (same), 40:50-56; '054 patent, 38:19-25, 42:3-6. The Court found that the term "memory module" has essential structural requirements not necessarily found in other modular computer accessories. *Id.* at 28 (noting explanation in Overview that "the invention 'is couplable to a memory controller of a host system,'" '918 patent at 3:66-67, i.e., not just the host system). The Court concluded that a POSITA would understand that a "memory module" is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. Ex. 7 at 28. Micron's own extrinsic evidence confirms this. In co-pending IPRs involving the '918/'054

patents, Samsung's expert Dr. Wolfe explained that, at the time of the inventions, "when we use the term memory modules, we typically were referring to main memory modules." Ex. 17 (Wolfe Deposition Tr. in IPR2022-00996) at 123:14-18 (distinguishing "memory modules" from "modules that contained memory" such as graphics cards).

B. Micron's New Claim Construction Arguments Should Be Rejected

1. "converter circuit" ('918 patent, all asserted claims)

Term	Netlist	Micron
"converter circuit"	Not subject to § 112, ¶ 6; plain and ordinary meaning, i.e., a circuit for voltage conversion	The "converter circuit" feature is subject to § 112, ¶ 6, with the corresponding functionality being the functions of: (i) "provid[ing] a fourth regulated voltage having a fourth voltage amplitude"; (ii) "reduc[ing] the pre-regulated input voltage to provide a fourth regulated voltage"; (iii) "provid[ing] the fourth regulated voltage"; and (iv) "reduc[ing] the pre-regulated voltage input to provide the fourth regulated voltage". The corresponding structure that is "configured to" perform the recited functions is a "converter circuit," as described in the '918 patent at 29:18–64.

As a preliminary matter, it is improper for Micron to require the functions recited in different claims to apply to all claims. For instance, claim 1 of the '918 patent does not require the claimed "converter circuit" to reduce a "pre-regulated input voltage" to provide a fourth regulated voltage.

The term "converter circuit" is also not subject to § 112, ¶ 6, which applies generally to claims drafted using means-plus-function language. "[T]he failure to use the word 'means' . . . creates a rebuttable presumption . . . that § 112, para. 6 does not apply." *Williamson v. Citrix Online LLC*, 792 F.3d 1339, 1348-49 (Fed. Cir. 2015) (*en banc*) (noting that the presumption is rebuttable only when the claim term fails to "'recite sufficiently definite structure' or else recites 'function without reciting sufficient structure for performing that function'"). "In the absence of the word 'means,'" Micron bears the burden of demonstrating "by a preponderance of the evidence that the ['converter circuit' limitation] fails to recite sufficiently definite structure." *Dyfan, LLC v. Target Corp.*, 28 F.4th 1360,

1370-71 (Fed. Cir. 2022). It cannot meet that burden here.

Specifically, Micron's expert Dr. Stone asserts that as used in the claims, a POSITA would understand the term "converter circuit" to be "a generic term that encompasses any hardware, software, or combination that may perform the claimed functions." Ex. 8 (Stone Decl.), ¶ 51; *see also id.*, ¶ 25 (POSITAs would know structures of voltage conversion and regulation circuitry). Dr. Stone ignores both the meaning of the "circuit" to a POSITA and that the claims include contextual language describing the operation and output of the "converter circuit." *See, e.g.*, '918 patent, 39:37-39 (cl. 13), 38:61-67 (cl. 5), 39:63-64 (cl. 16).

The word "circuit" is a well-known term in electronics that connotes structure, such as an "[a]rrangement of conductors and passive and active components forming a path, or paths, for electrical current." Ex. 18 (Chambers Dictionary of Science and Technology, 2007) at 224. Other contemporaneous dictionary definitions are in accord. *See, e.g.*, Ex. 19 (Comprehensive Dictionary of Electrical Engineering, 2005) at 112 (defining "circuit" as "a ***physical device*** consisting of an interconnection of elements . . . . For example, an electric circuit may be constructed by interconnecting a resistor and a capacitor to a voltage source."); Ex. 20 (Dictionary of Computing, 2008) at 78 (defining "circuit" as "[t]he combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some desired function"). In other words, a "circuit" connotes "sufficiently definite structure" and is not subject to § 112, ¶ 6. *See Estech Sys. IP, LLC v. Mitel Networks, Inc.*, No. 2:21-cv-473, 2023 WL 2695093, at *14 (E.D. Tex. Mar. 28, 2023) ("By reciting the objectives of the 'circuitry,' and how the circuitry operates within the context of the claimed invention, the claim language connotes sufficiently definite structure to one of skill in the art."). Indeed, Micron effectively concedes that the term "circuit" on its own is sufficient to connote structure, given that Micron is ***not*** proposing § 112, ¶ 6 treatment for the "first circuit" term of '054 claim 1. *See* Dkt. 69-2 at 32.

The Federal Circuit has also "previously held on several occasions that the term 'circuit' connotes structure" such that § 112, ¶ 6 does not apply. *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1364-65 (Fed. Cir. 2013) (citing *MIT v. Abacus Software*, 462 F.3d 1344, 1355 (Fed. Cir. 2006), *Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1320-21 (Fed. Cir. 2004), and *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1373 (Fed. Cir. 2003)). For example, in *Apex*, the Federal Circuit concluded that the term "circuit" recited sufficient structure in the context of the claims at issue. 325 F.3d at 1372-73 (considering the use of the term "circuit" in the claim limitation "a first interface circuit for receiving keyboard and cursor control device signals from the workstation"). Based on the above-quoted definition of the term "circuit" from the Dictionary of Computing, the court reasoned that "the term 'circuit' by itself connotes some structure." *Id.* at 1373. Moreover, the court observed that "the term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies some structural meaning to one of ordinary skill in the art." *Id.*

Here too, the claimed "circuit" as modified with the identifier "converter" identifies certain structural meaning to one of ordinary skill in the art, *i.e.*, a combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill a voltage conversion function. The claims further describe the circuit's operation within the context of the claimed memory module. For example, dependent claim 13 requires that the "converter circuit" be coupled to the "power input voltage" received via the "second portion of the plurality of edge connections" of the DIMM. '918 patent, 39:37-39 ("The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit."); *id.*, 38:61-67 ("The memory module of claim 1, further comprising: a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections . . . ."); *id.*, cl. 1 (converter circuit configured to provide a fourth regulated voltage having

a fourth voltage amplitude); *see also, e.g.*, *id.*, 39:63-64 (cl. 16) ("a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage").

Section 112, ¶ 6 does not apply where, as here, "the structure-connoting term 'circuit' is coupled with a description of the circuit's operation." *Linear Tech.*, 379 F.3d at 1320 (claim reciting "a first circuit for monitoring a signal from the output terminal to generate a first feedback signal" did not require § 112, ¶ 6 treatment because "[t]he contextual language describes the objective of the 'circuit' . . . and the desired output of the 'circuit'").

2. "first circuit" ('054 patent, claim 1-13, 15)

Term	Netlist	Micron
"first circuit"	plain and ordinary meaning	"a circuit that is different from a memory module controller"

Micron contends that the term "first circuit" in '054 claim 1 is "different from" a "memory module controller," but has provided no explanation of what it means by "memory module controller," a term not found anywhere in the '918/'054 patents. Nor has Micron provided any explanation of how a "memory module controller" differs from the "controller" that is recited in certain dependent claims that depend from claim 1. *E.g.*, '054 patent, cls. 5, 7, 8, 23, and 24.

Micron's construction finds no support in the claim language. Claim 1 of the '054 patent recites contextual language for the operation of the "first circuit." *See* '054 patent, 38:33-42 ("a plurality of components coupled to the PCB . . . the plurality of components including . . . a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections, wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages"). As discussed above, the term "circuit" has a well-understood definition to a POSITA. *See supra*, 18-21. The claim language provides all the context needed to understand the structure of the "first circuit," and construction of the term is therefore unnecessary.

The specification does nothing to alter the plain and ordinary meaning of this term. *Hill-Rom*,

755 F.3d at 1372 (plain and ordinary meaning applies absent "clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction'") (citations omitted). One example of a first circuit that meets the recitation for the "first circuit" of '054, cl. 1 is a circuit that comprises registers 1160 and switches 1170 as shown in Figure 15A. That combination receives one set of address/control signals and outputs another set. *See* '054 patent, Fig. 15A; Figs. 12-14 (the switch 1052 receiving address/control signals from either DIMM interface or controller 1062 and outputting address/control signals to DRAMs). It also receives two voltages, a Vdd for operating the registers 1160 and one for operating the switches 1170. *E.g.*, 29:39-54 (1.8V for Vdd and 2.5V or 3.3V for isolation devices), 25:48-51 (isolation switch FSA1208). Fig. 15A depicts "a registered DIMM subsystem." *Id.*, 23:41-44. These circuits control the memory module and therefore can be considered a "memory module controller." Micron's attempt to differentiate a "first circuit" from a "memory module controller" should be rejected.

3. "at least one circuit" ('918, cls. 1-3, 5-7, 9-13, 15, 21)

Term	Netlist	Micron
"at least one circuit"	Not subject to § 112(6); plain and ordinary meaning. If subject to §112(6), then: Function: (i) receive a first plurality of address and control signals via [the first/a second] portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices. Structures: As described in 21:14-23, 23:27-31, 23:41-24:8 or equivalents thereof.	The "at least one circuit" feature is subject to § 112, ¶ 6, with the corresponding functionality being the functions of: (i) "receiv[ing] a first plurality of address and control signals via the first portion of the plurality of edge connections"; (ii) "output[ting] a second plurality of address and control signals to the plurality of SDRAM devices"; (iii) "receiv[ing] a first plurality of address and control signals via a second portion of the plurality of edge connections"; and (iv) "output a second plurality of address and control signals to the plurality of SDRAM devices". The corresponding structure that is "operable to" perform the recited functions is a "circuit that is different from a memory module controller," as described in the '918 patent at 21:14–26:65, 29:33–54.

The term "at least one circuit" is also not subject to § 112, ¶ 6 because the limitation does not use the word "means" and Micron cannot overcome the presumption that § 112, ¶ 6 does not apply. As discussed above, the Federal Circuit has consistently found the term "circuit" connotes structure, and is not a nonce term. *See supra*, 18-21. Micron tacitly concedes that § 112, ¶ 6 does not apply to this term by not identifying the similar "first circuit" term for the '054 patent for means-plus-function treatment. The claims of the '918 patent provide further context for the "at least one circuit" that connote structure. Claim 1 requires the "at least one circuit" to be "coupled between a first portion of the plurality of edge connections [of the memory module] and the plurality of SDRAM devices," and further requires it to be "coupled to both the second regulated voltage and the fourth regulated voltage." '918 patent, 38:41-43, 38:47-49. The claim language also specifies the inputs to the "at least one circuit" (*i.e.*, the first plurality of c/a signals) and the outputs (*i.e.*, the second plurality of c/a signals). *Id.*, 38:43-47. Such contextual language provides further detail to connote structure and function of the claimed circuit to a POSITA. *See Linear Tech.*, 379 F.3d at 1320-21 (holding that the term "circuit" in a claim reciting "a first circuit for monitoring a signal" is not a means-plus-function limitation because the claim provided "a recitation of the respective circuit's operation in sufficient detail to suggest structure to persons of ordinary skill in the art"); *E2E Processing, Inc. v. Cabela's Inc.*, No. 2:14-cv-36, 2015 WL 4051423, at *6 (E.D. Tex. July 2, 2015) (Section 112 ¶ 6 does not apply when there is context as to the "inputs and outputs" and where the components "interact[] with other components . . . in a way that . . . inform[s] the structural character of the limitation-in-question or otherwise impart[s] structure").

If § 112, ¶ 6 applies, the Court should still reject Micron's proposed construction. First, as with the "converter circuit," Micron improperly aggregates functions from different claims and apply them to all claims. That improperly imports limitations from unrelated claims, and provides another

reason for rejecting Micron's proposed construction. Second, the corresponding structure includes: switch 1052 in Figs. 12-14 and/or register 1160 in Figs. 15A-C. *See* '918 patent, 21:14-23, 23:27-31, 23:41-24:8. For example, Figs. 12-14 depict the "at least one circuit" 1052 "Switch" receiving address/control signals (labeled "ADDR/CONT") from DIMM interface 1022 and transmitting address/control signals to SDRAMs 1032. *See* '918 patent, 21:14-23, 23:27-31.

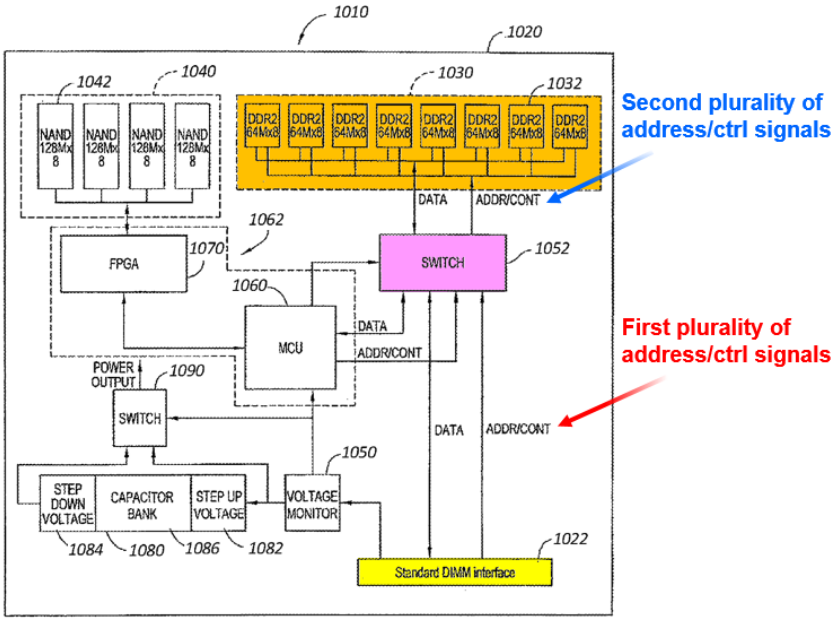


FIG. 12

The Court should also reject Micron's attempt to distinguish the recited "at least one circuit" from an undefined "memory module controller." To the contrary, the '918 patent teaches that one preferred embodiment of the invention may be in the form of "a registered DIMM" comprising "one or more registers 1160 and a plurality of DRAM elements 1180, as schematically illustrated by Fig. 15A." '918 patent, 23:41-44. As shown in Figure 15A, the register 1160 receives a plurality of input address/control signals from the system and outputs a plurality of address/control signals to the SDRAMs. Thus, the claimed at least one circuit can include all or part of the registers of an RDIMM, *i.e.*, the RCD that Micron is trying to exclude.[3]

[3] It can also additionally include additional switches and/or logic components.

4. "controller" ('918, cls. 12, 18-19, 25-26; '054, cls. 5, 7-13, 16-17, 23-25, 29-30)

Term	Netlist	Micron
"controller"	Not subject to § 112(6) and not indefinite; plain and ordinary meaning. To the extent that "controller" is a § 112(6) term, the function and corresponding structure vary for each claim, contrary to Micron's attempt to aggregate all functions into the term. Structures: ASIC, PLD, CPLD, FPGA, custom-designed semiconductor device as described in 23:1-27, 24:35-37, 25:8-31, 29:33-54, 32:49-51 or equivalents thereof.	**'918 patent** The "controller" feature is subject to § 112, ¶ 6, with the corresponding functionality being the functions of: (i) "receiv[ing] the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory"; (ii) "receiv[ing] the signal, wherein the controller executes a write operation in response to the signal"; and (iii) "receiv[ing] the signal, wherein, in response to the signal, the controller executes a write operation". The corresponding structure that is "configured to" perform the recited functions is a "controller that is different from the at least one circuit and the voltage monitor circuit and the one or more registers," as described in the '918 patent at 21:14–26:65, 29:33–54. **'054 Patent** The "controller" feature is subject to § 112, ¶ 6, with the corresponding functionality being the functions of: (i) "perform[ing] one or more operations including a write operation to transfer data to non-volatile memory" "in response to the trigger signal"; and (ii) "perform[ing] one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and wherein the one or more operations include a write operation to transfer data into non-volatile memory." The corresponding structure that is "configured to" perform the recited functions is a "controller that is different from the first circuit and the voltage monitor circuit," as described in the '054 patent at 21:14–26:65, 29:33–54.

The term "controller" is also not subject to § 112, ¶ 6 because the limitation does not use the word "means" and Micron cannot overcome the presumption that § 112, ¶ 6 does not apply. Courts have consistently held that the term "controller" is not subject to § 112, ¶ 6. *See, e.g.*, *Va. Innovation Scis., Inc. v. Amazon.com, Inc.*, No. 4:18-cv-474, 2019 WL 4259020, at *13 (E.D. Tex. Sept. 9, 2019);

Barkan Wireless IP Holdings, L.P. v. Samsung Elecs. Co., No. 2:18-CV-28, 2019 WL 497902, at *22-23 (E.D. Tex. Feb. 7, 2019). In *Barkan*, the court determined that the term "controller" in a claim requiring "a controller adapted to regulate data flow" was not subject to § 112, ¶ 6 because "[n]othing in the specification suggests that 'controller' lacks structure." 2019 WL 497902, at *22 (citing specification's disclosure that "[t]he channel electronic means 53 implements the actual communications to connect between the channels 51 and 52. A call controller 54 supervises and controls the operation of means 53"). The court also relied on technical dictionary definitions of "controller" that "reinforc[ed] that the term 'controller' refers to a known class of structures." *Id.*

Here too, nothing in the specification suggests that the term "controller" lacks structure. To the contrary, the specification refers to "controller 1062," which elsewhere is referred to by example as an FPGA. *See, e.g.*, '918 patent, 29:43-44 (referring to "the controller 1062 (e.g., an FPGA)"), 29:49-50, 23:22-27. This is a clear reference to a specific structure, and thus § 112, ¶ 6 does not apply. M*axell Ltd. v. Huawei Device USA Inc.*, 297 F. Supp. 3d 668, 748 (E.D. Tex. 2018) (declining to apply § 112, ¶ 6 to "controller" where "[t]he specification refers to 'controller 50' which elsewhere is referred to as 'external CPU 50,' a clear reference to specific structure"); *see also* '918 patent, 23:46-47 (controller can be a logic element), 23:1-27 (examples of logic element includes FPGA, PLD, ASIC, custom-designed semiconductor device, and CPLD). Multiple technical dictionary definitions also demonstrate that the term "controller" connotes structure. *E.g.*, Ex. 21 (Dictionary of Science and Technology, 2007) at 144 ("a device which ensures that something operates in the correct way"); Ex. 19 (Comprehensive Dictionary of Electrical Engineering, 2005) at 148 ("a unit that directs the operation of a subsystem within a computer"); *Barkan Wireless*, 2019 WL 497902, at *22 (quoting dictionary definitions of "controller"). Dr. Stone's declaration does not consider these well-known definitions of the term "controller," and thus his testimony should be given no weight. Ex. 8 (Stone Decl.) ¶¶ 57-60.

Even if § 112, ¶ 6 applies, Micron's attempt to aggregate the "function" of the claimed

"controller" under one construction is improper because it effectively imports limitations from one claim into another. *See* '918 patent, 39:31-36 (cl. 12), 40:17-21 (cl. 18), 42:1-5 (cl. 25); '054 patent, 38:65-39:3 (cl. 5), 39:15-20 (cl. 7), 39:21-29 (cl. 8), 40:13-20 (cl. 16), 41:1-4 (cl. 23).

Moreover, Micron's argument that the corresponding structure of the "controller" should be "different from" the "at least one circuit" ('918), "one or more registers" ('918), "first circuit" ('054), or "voltage monitor circuit" ('918/'054) should be rejected. Micron's injection of "different from" into the construction of this term would introduce more ambiguity than clarity and is inconsistent with the express language of the claims at times. For example, the specification teaches that the voltage monitor circuit can be part of, or separate from, the controller, which is also suggested by the claim language. '918 patent, 25:27-31; *compare* '054, cl. 7 ("a controller coupled to the voltage monitor circuit") *with* cl. 8 ("the controller including a voltage monitor circuit . . . ."). As another example, the specification teaches that the controller can include memory components "which stores configuration information to program the FPGA." '918 patent, 23:24-27. Registers can be used to store configuration information. As a result, the controller can include registers. As a further example, Fig. 15C shows the at least one circuit 1052 to be part of the FPGA controller 1070. *See* Fig. 15C, 23:64-24:3 ("As schematically illustrated by Fig. 15C, in certain embodiments the at least one circuit 1052 comprises a dynamic on-die termination (ODT) 1176 circuit of the logic element 1070 . . . ."); 23:46-47 (controller 1062 (e.g., logic element 1070)"). Micron's proposal should therefore be rejected.

5. "first operable state"/"second operable state" ('054 patent, cls. 4-7, 11-12, 16-17, 23, and 25)

Term	Netlist	Micron
"first operable state"	"first operable state" is a "state in which the memory module is operated before transition"; not indefinite	"state in which a controller and a non-volatile memory subsystem are operatively decoupled (e.g., isolated) from a volatile memory subsystem by at least one circuit"; or in the alternative, indefinite.
"second	"second operable state" is	"state in which the volatile memory subsystem is

operable state"	a "state in which the memory module is operated after transition"; not indefinite	operatively coupled to the controller to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller"; or in the alternative, indefinite

Netlist proposes adopting the constructions of the "operable state" terms that Samsung and Netlist previously agreed to. *Samsung I*, Dkt. 70 at 2. Micron argues that the claims should be limited to particular types of "operable states" defined by whether the non-volatile memory subsystem is operatively coupled to the volatile memory subsystem. But that is not what is claimed: The claim language clearly indicates that the "operable state" refers to the state of the memory module. *E.g.*, '918 patent, 40:19-20 (cl. 16) ("the ***memory module*** transitions from a first operable state to a second operable state"), 38:62-64, 39:12-14, 39:46-47, 42:5-6. So too does the Court's holding that the preamble ("A memory module") is limiting. Ex. 7 at 35. Certain claims also require that the memory module transition from a "first operable state" to a "second operable state" in response to detecting an amplitude change in the input voltage level or a certain input voltage level. *E.g.*, *id.*, 40:17-20 (cl. 16) ("in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state"); *id.*, 38:55-64 (cl. 4) ("the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal"). The "first operable state" thus simply refers to the state in which the memory module was operated before transition, and the "second operable state" likewise refers to the state in which the memory module was operated after transition. No further construction is necessary.

The specification likewise supports Netlist's construction. For example, the specification refers to the "first state" as the state of the memory module in the absence of a trigger condition such as a power failure. *See, e.g.*, '054 patent, 25:58-60 ("In certain embodiments, the memory system 1010

is in the first state when no trigger condition (e.g., a power failure) is present . . . ."); *see also, e.g.*, *id.*, 27:4-5 (referring to the "first state" as the state "after power is restored" following a trigger condition). Likewise, the specification refers to the "second state" (or "third state," in some embodiments) as a state in response to a trigger condition. *See, e.g.*, *id.*, 25:3-7 ("The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up."); 25:54-62; 26:38-43 (referring to power down as an example of the "second state"), 28:39-58 (noting that in certain embodiments, "power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition ***has occurred***"), Fig. 17 (change in state machine for different conditions). Netlist's construction is consistent with the specification.

Micron's construction would limit the "operable state" terms to only "certain embodiments" in the specification, and is thus improper. *See* '054, 24:60-25:7 ("The memory system 1010 ***of certain embodiments*** is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062."); 25:62-26:3 ("***In certain embodiments***, the memory system 1010 has a third state in which the controller 1062 is operatively decoupled from the volatile memory subsystem 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). For example, in one embodiment the third power supply may provide power to the volatile memory subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred.").

These are simply examples, and do not limit the clear language of the claims. Even worse, Micron's construction introduces unclaimed elements, such as the "at least one circuit" that appears nowhere in the claims. *E.g.*, '054, cl. 16. That is improper.

Micron argues that, if its constructions are not adopted, the claims are indefinite. "[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). "[A] patent must be precise enough to afford clear notice of what is claimed," but that consideration must be made while accounting for the inherent limitations of language. *Id.* at 908-09.

During meet and confer, Micron suggested that Netlist's interpretation of the "first operable state" and "second operable state" terms in *Samsung I* was overbroad, and thus indefinite. But "the inference of indefiniteness simply from the scope finding is legally incorrect: 'breadth is not indefiniteness.'" *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1367 (Fed. Cir. 2017) (citation omitted). The claim language provides context for both the "first operable state" and the "second operable state" in relation to the level of the input voltage, requiring the memory module to transition from the "first operable state" to the "second operable state" in response to the input under or over-voltage detection. '054 patent, 38:55-64, 39:4-14, 40:17-20, 42:3-6. So too does the specification. *See id.*, 25:58-60, 25:3-7, 25:54-62; 25:62-26:3, 26:38-43, 27:4-5, 28:39-58. Thus, Micron cannot carry its burden to prove by clear and convincing evidence that, if its constructions are not adopted, the claims are indefinite. *See Personalized Media Commc'ns, LLC v. Apple, Inc.*, No. 2:15-cv-01206, 2016 WL 6299860, at *42-43 (E.D. Tex. Oct. 26, 2016) (terms "first passing fashion" and "second passing fashion" held not indefinite where "[t]he specification provides numerous details regarding ways portions could be passed," and thus it was "reasonably certain that, as claimed, there merely must be a first fashion and a second fashion"); *Sonix*, 844 F.3d at 1377.

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CERTIFICATE OF SERVICE

I hereby certify that, on June 7, 2023, a copy of the foregoing was served to all counsel of record.

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